

Fig. 1A

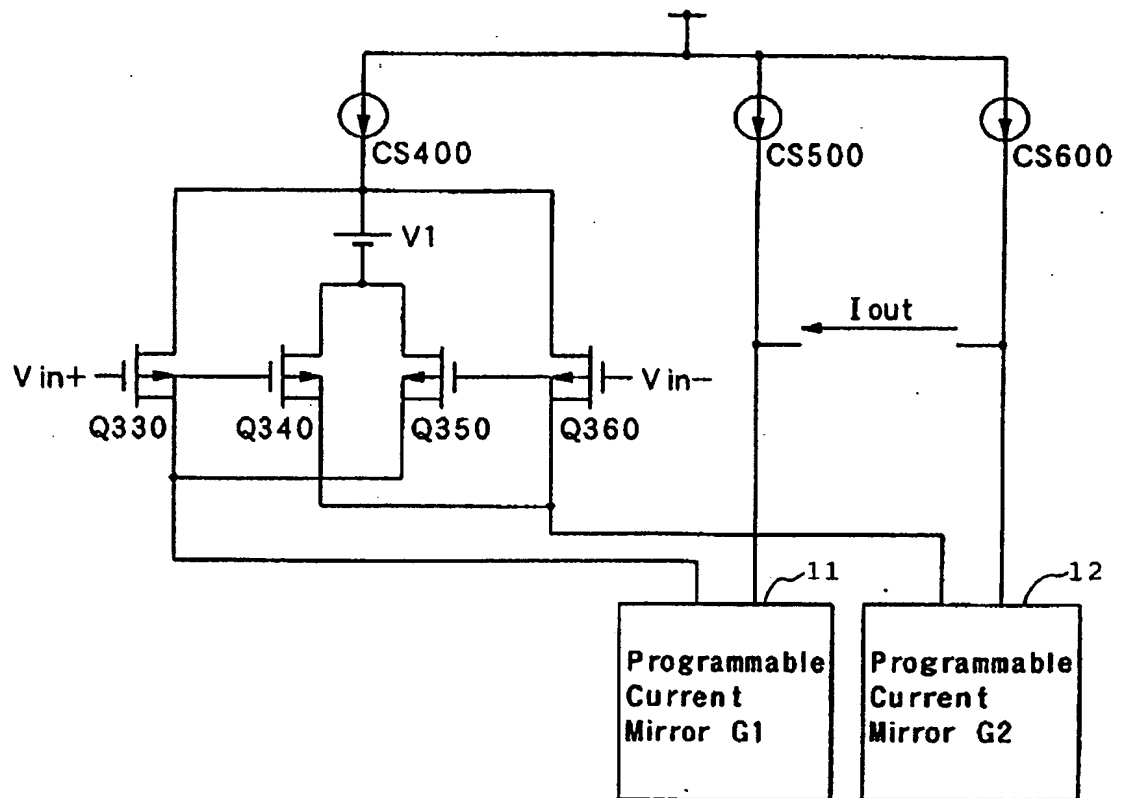


Fig. 1B

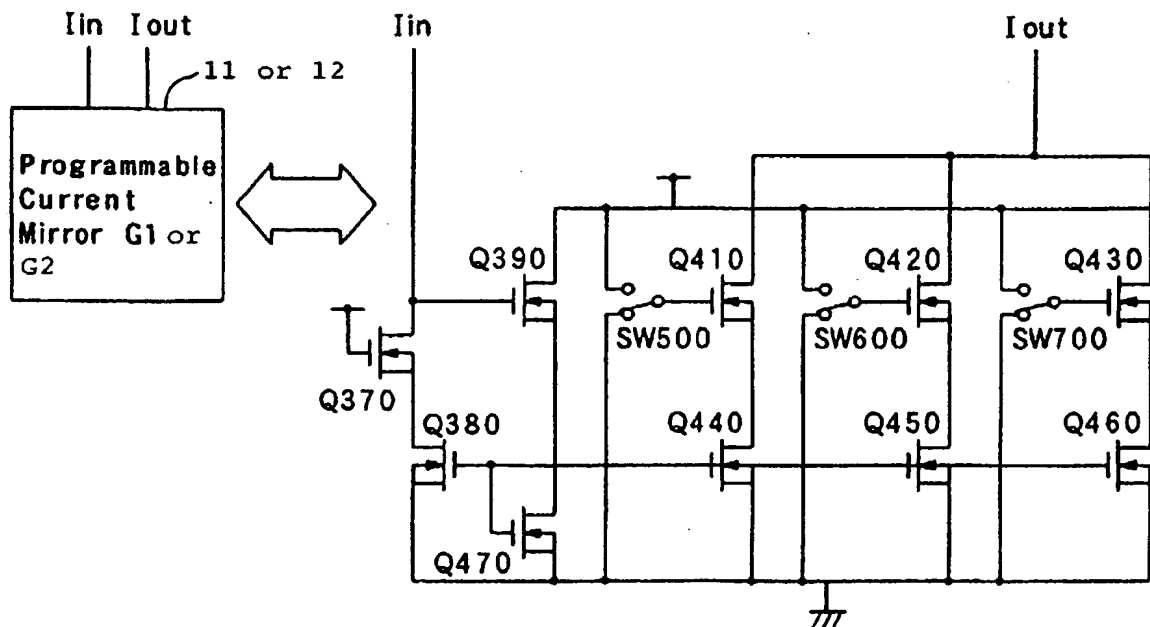


Fig. 2

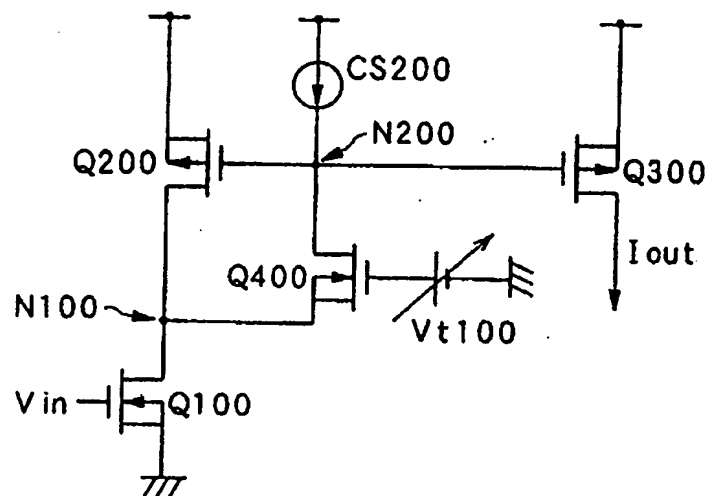


Fig. 3A

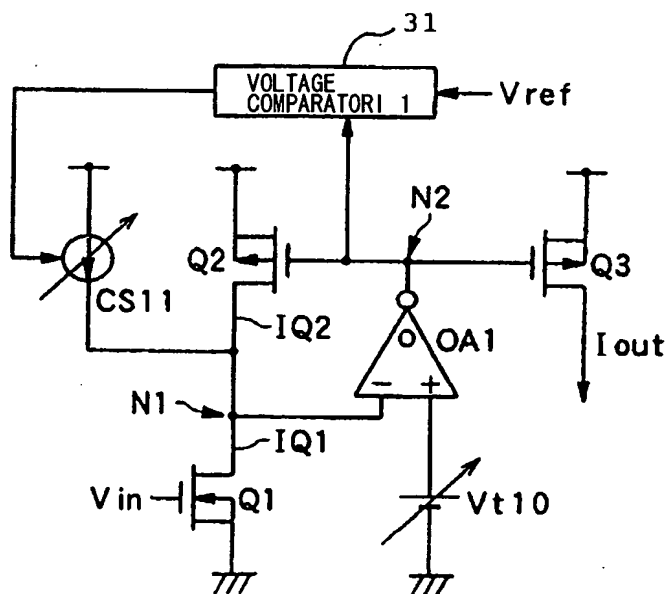


Fig. 3B

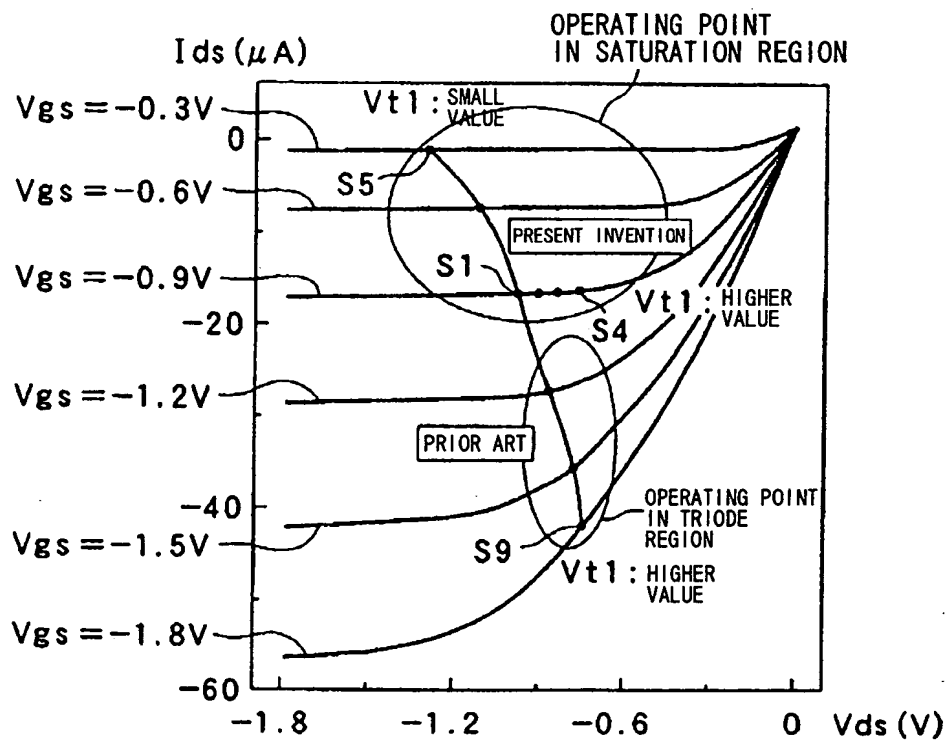


Fig. 4

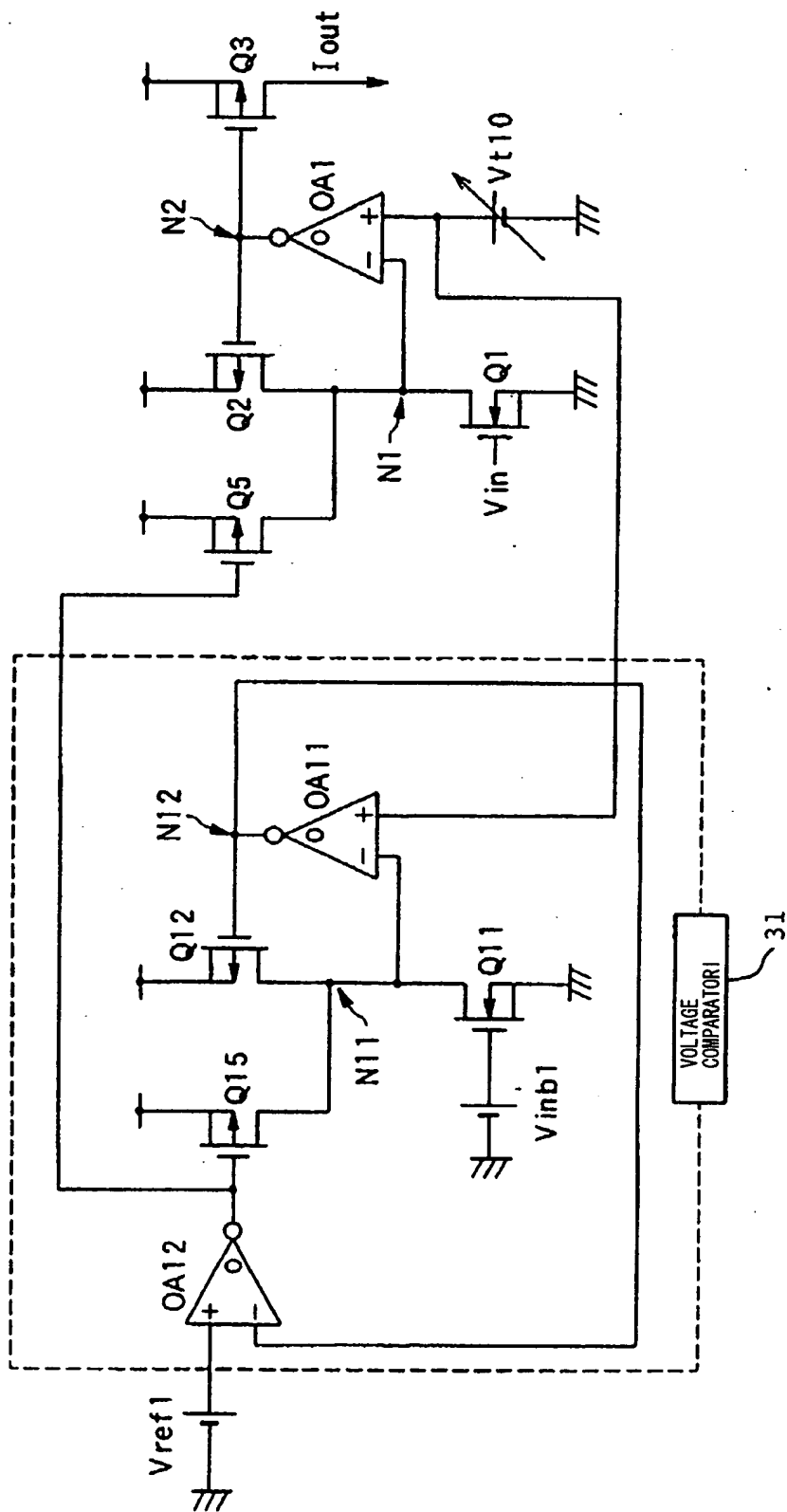
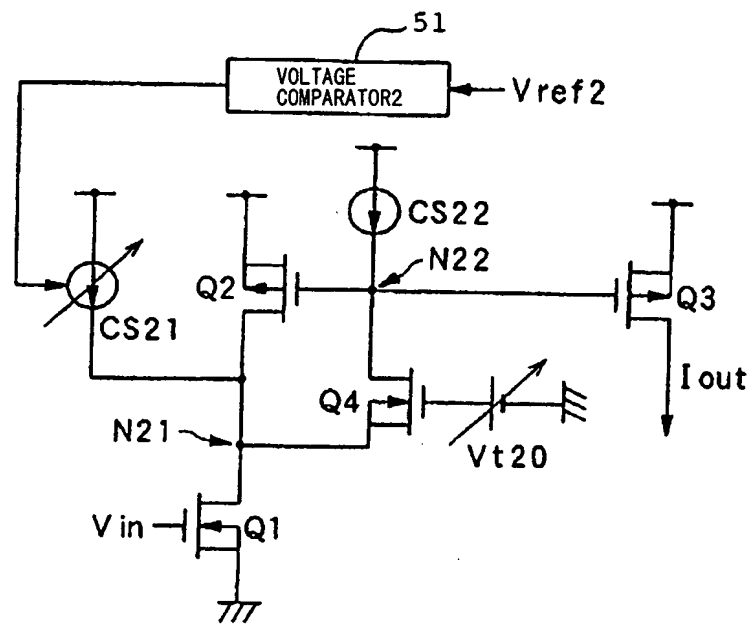
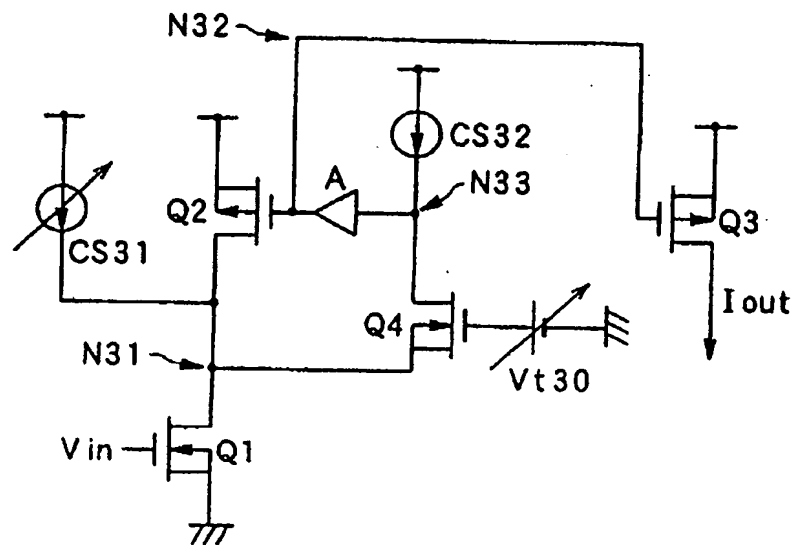


Fig. 5



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Fig. 7



The circuit diagram of voltage comparator 81 includes a differential amplifier stage. The input stage consists of a PMOS network with transistors Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q30, Q31, Q32, Q33, Q34, Q35, Q36, Q37, Q38, Q39, and Q40, and an NMOS network with transistors Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31, Q32, Q33, Q34, Q35, Q36, Q37, Q38, Q39, and Q40. The output of the differential amplifier is connected to the inputs of the voltage comparator 81. The voltage comparator 81 is a block that compares the two input voltages and produces a digital output signal.



Figure 1 is a graph showing the relationship between  $V_{t40}$  (V) and current. The graph is divided into a SATURATION REGION on the left and a TRIODE REGION on the right. A dashed line represents the 'ADJUSTING RANGE OF PRIOR ART', and a solid line with diagonal hatching represents the 'ADJUSTING RANGE OF PRESENT INVENTION'. The solid line is labeled VN42 (PRESENT INVENTION) and VN41- $|V_{th}|$ . The dashed line is labeled VN42 (PRIOR ART).

The circuit diagram illustrates a 10-bit digital-to-analog converter (DAC) architecture. It is divided into two main sections: a top section for the current mirror array and a bottom section for the op-amp buffers.

**Top Section (Current Mirror Array):**

- A 10-bit digital input  $V_{in}$  is connected to the gates of a series of NMOS transistors  $Q1$  through  $Q10$ .
- Each  $Q_i$  is part of a current mirror pair with a PMOS transistor  $Q_{i+10}$  (e.g.,  $Q1$  and  $Q11$ ,  $Q2$  and  $Q12$ , etc.).
- The PMOS transistors  $Q_{i+10}$  are connected to a common PMOS load node, which is also connected to a reference current source  $I_{ref}$  (represented by a triangle with a diagonal line and  $V_{t40}$ ).
- The NMOS transistors  $Q_i$  are connected to a common NMOS load node, which is also connected to a reference current source  $I_{ref}$  (represented by a triangle with a diagonal line and  $V_{t40}$ ).
- The output current  $I_{out}$  is the sum of the currents from the NMOS transistors  $Q_i$ .

**Bottom Section (Op-Amp Buffers):**

- The output current  $I_{out}$  is converted to a voltage by a resistor network.
- This voltage is buffered by a chain of op-amp buffers:  $OA43$ ,  $OA45$ ,  $OA44$ , and  $OA46$ .
- Each op-amp buffer is configured as a voltage follower (buffer).
- The final output voltage  $V_{out}$  is taken from the output of the last buffer,  $OA46$ .
- Reference voltages  $V_{ref41}$  and  $V_{DD}$  are used for biasing and level shifting.

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Fig. 11

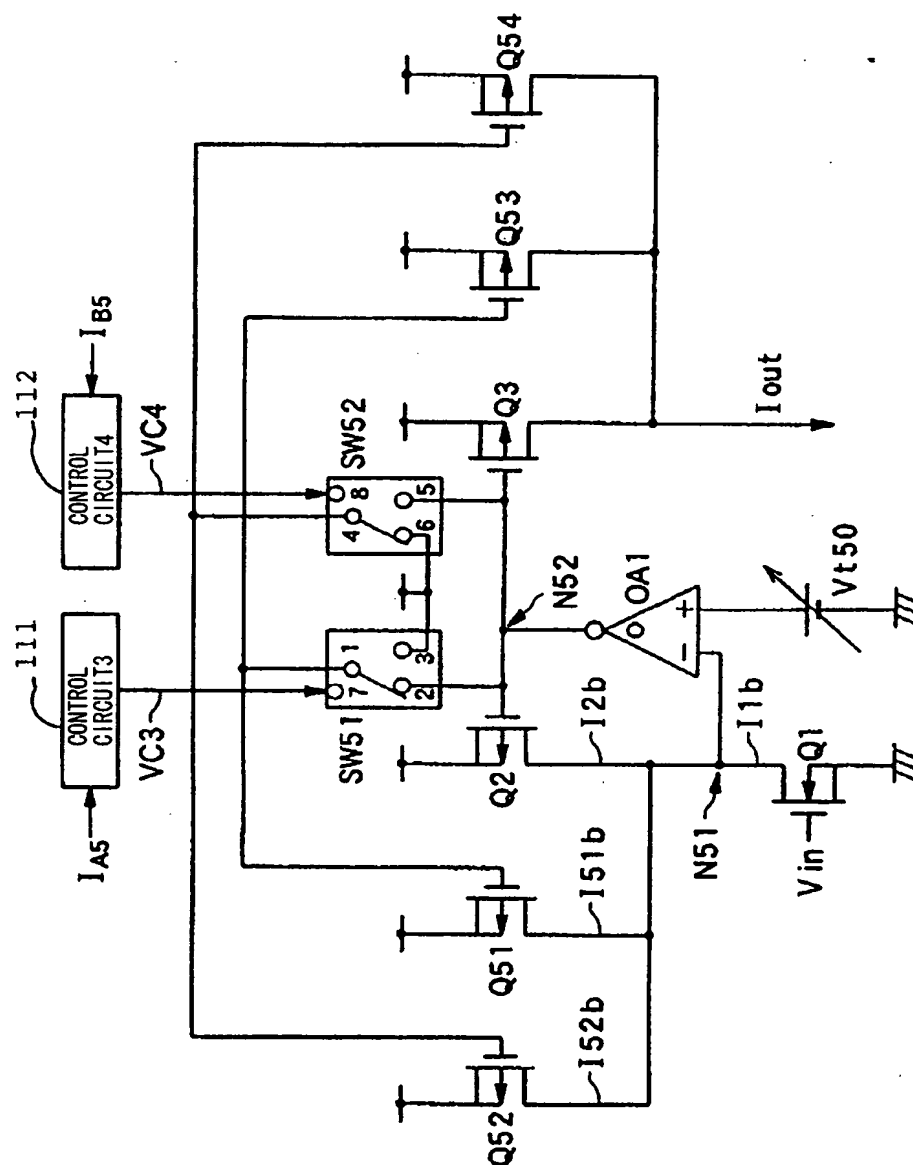


Fig. 12

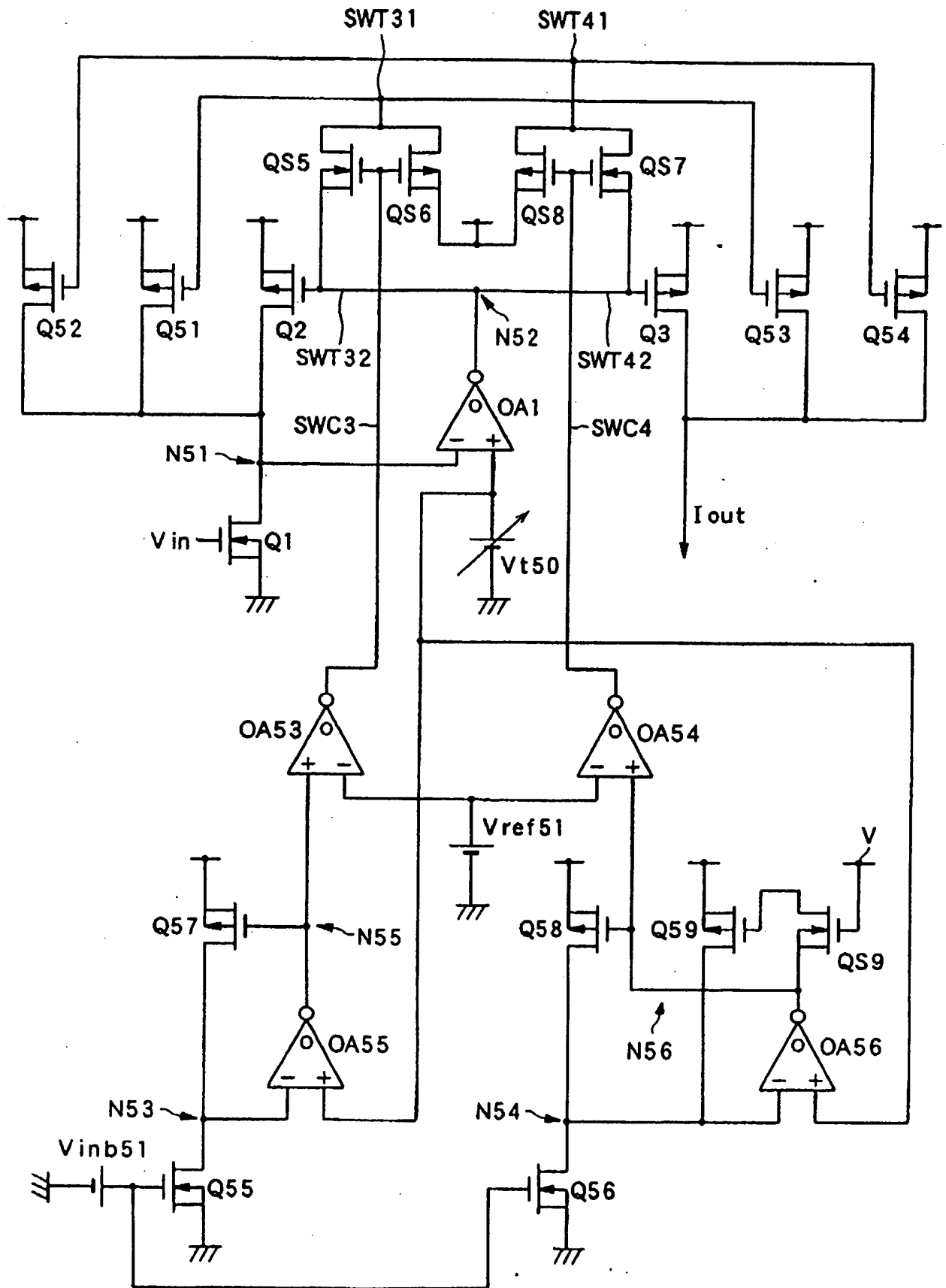


Fig. 13A

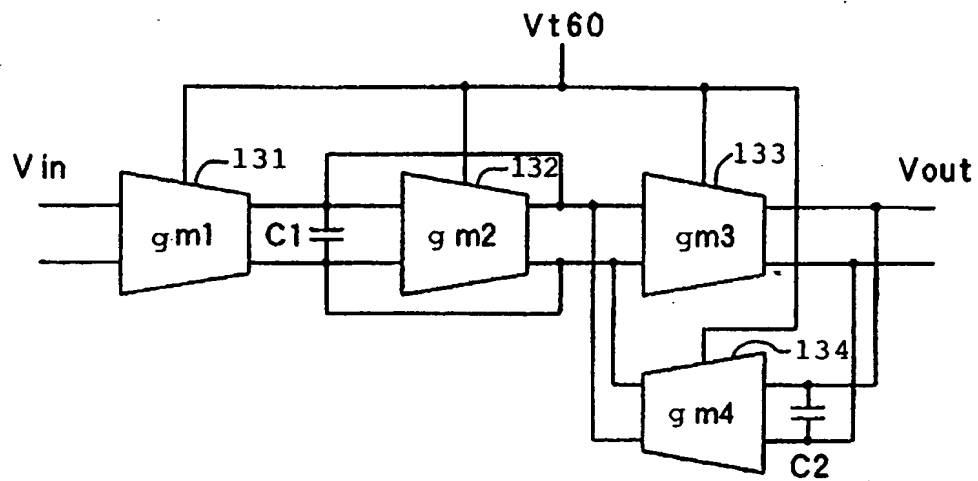


Fig. 13B

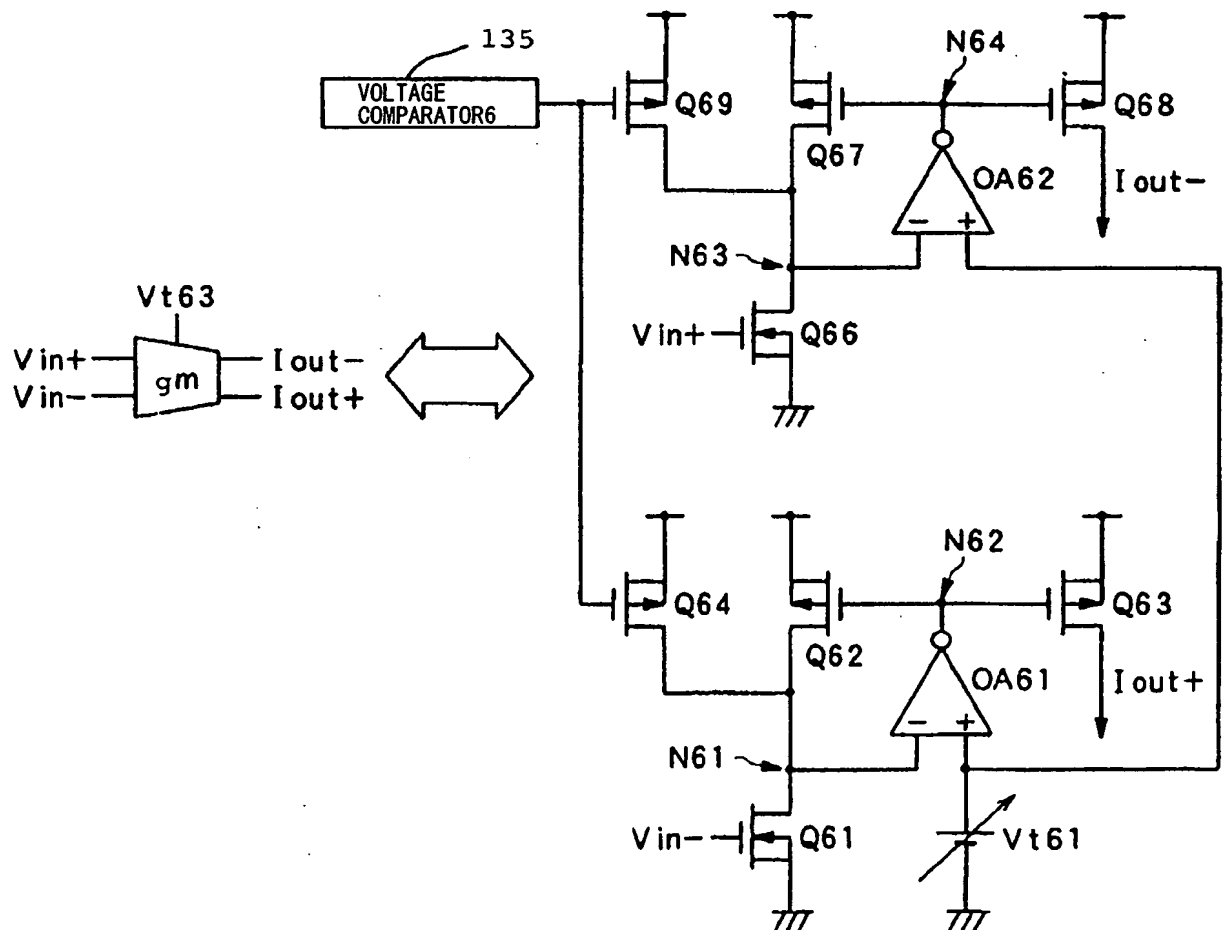


Fig. 14

